CLAIMS

1. A bond pad structure for an integrated circuit, comprising:

first and second active devices formed in a substrate;

first and second buses above the first and second active devices, respectively;

a bond pad above the first and second buses;

first interconnections between the first and second active devices and the bond pad; and

second interconnections between the first and second active devices and the first and second buses, respectively.

2. A bond pad structure as defined in claim 1, wherein said first active device comprises at least one PMOS transistor and said second active device comprises at least one NMOS transistor.

3. A bond pad structure as defined in claim 2, wherein the PMOS and NMOS transistors each include two or more connected source fingers, two or more connected drain fingers and two or more connected gate fingers.

4. A bond pad structure as defined in claim 2, wherein said first bus comprises a power supply bus and wherein said second bus comprises a power return bus.

5. A bond pad structure as defined in claim 4, wherein said first and second buses connect to a plurality of bond pad structures on an integrated circuit chip.

6. A bond pad structure as defined in claim 2, wherein the PMOS and NMOS transistors each include source, drain and gate fingers which are elongated in a direction of current flow in the first and second buses and which are narrow perpendicular to the direction of current flow.

7. A bond pad structure as defined in claim 2, wherein conductive islands are formed in the first and second buses for connection of the bond pad to the PMOS and NMOS transistors.

8. A bond pad structure as defined in claim 7, wherein the conductive islands are elongated in a direction of current flow in the first and second buses and are narrow perpendicular to the direction of current flow.

9. A bond pad structure as defined in claim 7, wherein each of the first interconnections comprises a plurality of individual contacts between the bond pad and the conductive islands and between the conductive islands and the active devices.

10. A bond pad structure as defined in claim 9, wherein the contacts between a first pair of adjacent levels are laterally offset relative to the contacts between a second pair of adjacent levels.

11. A bond pad structure as defined in claim 2, wherein the PMOS and NMOS transistors are configured as electrostatic discharge protection devices.

12. A bond pad structure as defined in claim 1, wherein said first active device comprises two or more PMOS transistors and said second active device comprises two or more NMOS transistors.

13. A bond pad structure as defined in claim 3, further comprising a guard band region formed in the substrate.

14. A bond pad structure as defined in claim 13, wherein said guard band region comprises an N+ guard band in an N-well for isolation of the PMOS transistor, a P+ guard band for isolation of the NMOS transistor and conductive interconnects between the power supply bus and the N+ guard band and between the power return bus and the P+ guard band.

15. A bond pad structure as defined in claim 14, wherein in the N+ guard band surrounds the PMOS transistor and the P+ guard band surrounds the NMOS transistor.

16. A bond pad structure as defined in claim 2, wherein the PMOS and NMOS transistors are interconnected in a CMOS configuration.

17. A bond pad structure as defined in claim 2, further comprising a metal level for connections to the gates of the PMOS and NMOS transistors.

18. A bond pad structure as defined in claim 2, wherein the first interconnections comprise connections between the bond pad and the drains of the PMOS and NMOS transistors.

19. A bond pad structure as defined in claim 4, wherein the second interconnections comprise a connection between the power supply bus and the source of the PMOS transistor.

20. A bond pad structure as defined in claim 19, wherein the second interconnections comprise a relatively wide source contact layer and distributed connections to the power supply bus.

21. A bond pad structure as defined in claim 4, wherein the second interconnections comprise a connection between the power return bus and the source of the NMOS transistor.

22. A bond pad structure as defined in claim 21, wherein the second interconnections comprise a relatively wide source contact layer and distributed connections to the power return bus.

23. A bond pad structure as defined in claim 9, wherein the contacts between adjacent levels of the structure are distributed over the conductive islands.

24. A bond pad structure as defined in claim 1, wherein the bond pad includes two or more spaced-apart bond pad layers.

25. A bond pad structure as defined in claim 24, wherein the two or more bond pad layers are interconnected by a plurality of individual contacts within a passivation opening associated with the bond pad structure.

26. A bond pad structure as defined in claim 24, wherein the two or more bond pad layers are interconnected by contacts located outside a passivation opening associated with the bond pad structure.

27. A bond pad structure as defined in claim 1, wherein the bond pad comprises a single, relatively thick metal layer.

28. A bond pad structure for an integrated circuit, comprising:
an active device formed in a substrate;
a power bus above the active device;

a bond pad above the power bus;

a first interconnection between the active device and the bond pad; and

a second interconnection between the active device and the power bus.

29. A bond pad structure as defined in claim 28, wherein the active device comprises at least one MOS transistor.

30. A bond pad structure as defined in claim 29, wherein the at least one MOS transistor includes source, drain and gate fingers which are elongated in a direction of current flow in the power bus and which are narrow perpendicular to direction of current flow.

31. A bond pad structure as defined in claim 28, wherein the active device comprises at least one silicon controlled rectifier.

32. A bond pad structure as defined in claim 28, wherein the active device comprises at least one electrostatic discharge protection device.

33. A method for fabricating a bond pad structure for an integrated circuit, comprising:

forming first and second active devices in a substrate;

forming first and second buses above the first and second active devices, respectively;

forming a bond pad above the first and second buses;

interconnecting the first and second active devices and the bond pad; and

interconnecting the first and second active devices and the first and second buses, respectively.

34. A method as defined in claim 33, wherein forming first and second active devices comprises forming at least one PMOS transistor and at least one NMOS transistor, respectively.

35. A method as defined in claim 34, wherein forming at least one PMOS transistor and at least one NMOS transistor comprises forming PMOS and NMOS transistors that each include source, drain and gate fingers which are elongated in a direction of current flow in the first and second buses and which are narrow perpendicular to the direction of current flow.

36. A method as defined in claim 34, further comprising forming conductive islands in the first and second buses for connection of the bond pad to the PMOS and NMOS transistors.

37. A method as defined in claim 36, wherein forming conductive islands comprises forming conductive islands that are elongated in a direction of current flow in the first and second buses and are narrow perpendicular to the direction of current flow.

38. A method as defined in claim 35, further comprising forming a guard band region in the substrate.

39. A method as defined in claim 38, wherein forming the guard band region includes forming an N+ guard band surrounding the at least one PMOS transistor and forming a P+ guard band surrounding the at least one NMOS transistor.

40. A method for fabricating a bond pad structure for an integrated circuit, comprising:

forming an active device in a substrate;
forming a bus above the active device;
forming a bond pad above the bus;
interconnecting a first terminal of the active device and the bond pad; and
interconnecting a second terminal of the active device and the bus.

41. A method as defined in claim 40, wherein forming an active device comprises forming at least one MOS transistor.

42. A method as defined in claim 41, wherein forming at least one MOS transistor comprises forming at least one MOS transistor including source, drain and gate fingers which are elongated in a direction of current flow in the bus and which are narrow perpendicular to the direction of current flow.

43. A method as defined in claim 40, wherein forming an active device comprises forming at least one silicon controlled rectifier.

44. A method as defined in claim 40, wherein forming an active device comprises forming at least one electrostatic discharge protection device.

45. A bond pad structure for an integrated circuit, comprising:
first and second circuit areas on a substrate;
a guard band region formed in the substrate;
first and second buses above the first and second circuit areas, respectively;
a bond pad above the first and second buses;
at least one first interconnection between circuitry in one or both of the first and second circuit areas and the bond pad; and

at least one second interconnection between circuitry in one or both of the first and second circuit areas and the first and second buses.

46. A bond pad structure as defined in claim 45, further comprising at least one PMOS transistor in the first circuit area and at least one NMOS transistor in the second circuit area.

47. A bond pad structure as defined in claim 46, wherein the PMOS and NMOS transistors comprise an electrostatic discharge protection circuit.

48. A bond pad structure as defined in claim 45, further comprising at least one silicon controlled rectifier in the first circuit area, wherein the second circuit area comprises an isolation area.

49. A bond pad structure as defined in claim 48, further comprising a guard band region surrounding the silicon controlled rectifier.

50. A bond pad structure as defined in claim 48, wherein the silicon controlled rectifier is configured for protecting an output of a circuit.